R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

IN THE DRAWINGS

While Applicant's representative does not necessarily agree with the requirement to label FIGS. 1 and 2, in order to further prosecution, FIGS. 1 and 2 have been labeled "conventional". Replacement FIGS. 1 and 2 are submitted herewith. As such, the objection to the drawings should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 16 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-10 under 35 U.S.C. §102 as being anticipated by Scheck '719 has been obviated by appropriate amendment and should be withdrawn.

Scheck discloses a system and method for reducing clock skew sensitivity of a shift register (Title).

In contrast, claim 1 of the present invention provides an apparatus comprising one or more groups of boundary scan cells, one or more group buffers, one or more repeater buffers and a

controller. The group buffers may be coupled to each of the groups of boundary scan cells. The repeater buffers may be coupled in series with the group buffers. The controller may be coupled to the groups of boundary scan cells through the group buffers and the repeater buffers. The apparatus may be configured to buffer the groups of boundary scan cells to reflect an order of I/Os around the apparatus and said groups of boundary scan cells are routed within an I/O portion of said apparatus to avoid routing through an interior portion of said apparatus. Claim 10 provides similar limitations.

In contrast, Scheck does not provide such an arrangement. In particular, FIG. 1 of Scheck (cited by the Examiner) is silent regarding where the I/Os are placed. FIG. 4 of Scheck shows that the controller 402 is in the center (or interior portion) of the apparatus. In contrast, the claimed invention places the repeat buffers around the outside of the apparatus (the I/O portion), avoiding routing in the center portion. Furthermore, Scheck does not appear to make a distinction between the repeat buffers (e.g., 106a-106n, the claimed repeated buffers) and the circuits (104a-104n, the claimed one or more group buffers). Therefore, Scheck is silent regarding a number of the claimed elements and the rejection should be withdrawn.

Furthermore, claim 6 is believed to be independently patentable over Scheck. In particular, claim 6 provides that each boundary scan cell of said groups of boundary scan cells are implemented within an I/O cell. Fisher is silent regarding

implementing boundary scan cells within an I/O cell, as in presently claimed claim 6. Therefore, claim 6 is independently patentable over Scheck and the rejection should be withdrawn.

The rejection of claim 11 under 35 U.S.C. §102 as being anticipated by Fisher '928 has been obviated by appropriate amendment and should be withdrawn.

Fisher discloses a system and method for generating integrated circuit boundary register description data (Title).

In contrast, claim 11 of the present invention provides a method for optimizing buffers for JTAG boundary scan nets, comprising the steps of (A) reading a netlist, (B) reading an I/O order list, (C) defining a number of I/Os per groups, (D) determining if a last I/O is connected, and (E) writing a final netlist.

Fisher does not disclose or suggest each and every step of claim 11. In particular, the Examiner asserts that Step (D), which reads, "determining if a last I/O is connected" is taught by column 9, lines 21-29 of Fisher. However, the cited passage of Fisher merely states that "traversing said at least one hierarchal netlist for at least one individual netlist describes at least one pad located within said integrated circuit". It is unclear how this involves determining if the last I/O is connected. Clarification is requested or the rejection should be withdrawn.

Furthermore, claims 12-17 are believed to be independently patentable over Fisher. In particular, Fisher appears silent regarding "determining if starting a new group is

necessary", as in claim 12, "splitting a net" as in claim 13, "inserting a repeater buffer" as in claim 14, "inserting a group buffer" as in claim 15, "connecting a next I/O to a newest group buffer", and/or repeating Step (D) as in claim 17. Furthermore, based on a word search, Fisher does not even contain many of the key words of the dependent claims. In particular, Fisher does not even contain the word "splitting". Therefore, claim 13 should be fully patentable over Fisher. Fisher does not contain the phrase "new group". Therefore, claim 12 should be patentable over Fisher. Fisher does not contain the word "inserting" or the word "repeater". Therefore, claim 14 should be fully patentable over Fisher. Fisher does not contain the phrase "group buffer". Therefore, claim 15 and 16 should be fully patentable over Fisher. As such, claims 12-17 are believed to be independently patentable over Fisher.

As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 12-20 under 35 U.S.C. §103 as being unpatentable over Fisher '923 in view of Scheck '719 has been obviated by appropriate amendment and should be withdrawn. Claims 12-20 depend, directly or indirectly, from claim 11, which is now believed to be allowable.

As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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